REMARKS

This is in response to the Office Action mailed February 25, 2004. Applicant respectfully traverses and request reconsideration.

Examiner Telephone Interview

Applicant's attorney extends gratitude to Examiner Tran and Primary Examiner Cuneo for niceties extended during a March 16, 2004 telephone interview. Agreement was reached regarding potential clarifying amendments which would be outside the scope of a proper after final response, thereby necessitating further prior art searching by Examiner Tran. Further, the discussion provided insight into the Examiner's interpretations of claims limitations as applicable to the teachings of the prior art. In response to the discussion, Applicant herein submits claim amendments within the permissible boundaries of the After Final response, thereby not necessitating further prior art searching by Examiner Tran.

Claim amendments

Applicant respectfully submits that the submitted amendments adding claims 27 and 28-31 are proper in view of the present After Final response. Claim 27 presents the combination of previously presented limitations of claims 15, 16 and 17. Claim 17 originally depended from claim 16 which originally depended from claim 15, therefore added claim 27 does not present any new subject matter and is merely as to form and not to substance. Similarly, claims 28-31 recite a product by process claim, in accordance with MPEP §2173.05(p) reciting limitations previously found within existing claims 23-26.

Therefore, it is submitted the present amendments are proper and entrance of these amendments would not require the Examiner to conduct further searching as these amendments do not add any new subject matter beyond the originally presented claimed subject matter. Entrance and examination of the presently submitted claims is respectfully requested.

Rejection Under 35 U.S.C. §112, ¶2

Claim 20 currently stands rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. In view of the cancellation of claim 20, this rejection is submitted as being moot.

Rejection Under 35 U.S.C. §103(a)

A. Claims 1-7, 15-16 and 18-22

Claims 1-7, 15-16 and 18-22 currently stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dockerty et al., U.S. Patent No. 5,796,169 (hereinafter refereed to as "Dockerty") in view of Matthies et al., U.S. Patent No. 6,527,159 (hereinafter referred to as "Matthies").

In view of the cancellation of claims 1-7, 15-16 and 20-22, this rejection is submitted as being moot. Regarding claims 18 and 19, Applicant will address these claims in view of added claim 27 below.

B. Claims 8-14, 17 and 23-26

Claims 8-14, 17 and 23-26 currently stand rejected under 35 U.S.C. §103(a) as being unpatentable over Dockerty in view of Burnette, U.S. Patent No. 5,956,606 (hereinafter referred to as "Burnette").

Regarding claims 8-14, this rejection is submitted as being moot. Regarding claims 23-26, Applicant will address these claims after first addressing the rejection of claim 17, currently pending claim 27.

Pending claims 18-19, 23-26 and 27

Claim 27 recites limitations originally found within claim 17, therefore Applicant will address claim 27 in view claim 17 standing rejected as being obvious under 35 U.S.C. §103(a) over Dockerty in view of Burnette.

Originally, claim 17 is rejected based on the rejection of limitations recited in previously pending claim 10 in conjunction with the second solder balls. Claim 27 recites, among other things, "the substrate further includes an application specific integrated circuit disposed on the bottom surface of the carrier substrate." In the present rejection, the Examiner has asserted the carrier substrate as element 1, illustrated in FIGS. 1 and 5. This element is clearly labeled in FIG. 5 as being a printed circuit board, as well as being supported by the specification, see for example Col. 3, line 56.

On page 6 of the present rejection, the final paragraph on Page 6 states that "[w]ith respect to claim 10, figure 1 of Dockerty et al further shows that integrated circuit (3) disposed on the bottom side of the carrier substrate (1)." Therefore, for the Examiner's rejection to be proper in claim 27, by implication, the application specific integrated circuit is taught by the integrated circuit (3).

Claim 27 further recites that the first solder balls create the solder joints between the top surface (printed circuit board) and the bottom surface (carrier substrate) and that the second solder balls define a minimum distance between the carrier substrate and the printed circuit board. Herein, the Examiner asserts obviousness of one having ordinary skill in the art would utilize the bumping and packaging semiconductor die of Burnette to created the claimed invention, specifically the balls 314 and 318 of FIG. 11.

Applicants submit that combining Burnette and Dockerty fails to produce the claimed present invention because, *inter alia*, the solder balls 314 of Burnette do not create solder joints and the solder balls 318 of Burnette do not define a minimum distance between the carrier substrate and the printed circuit board. Burnette does not disclose the solder balls 314 and 318 being of different melting temperatures. Therefore, assuming one took the teaching of different melting temperatures from Dockerty, the first solder 314 creates a solder joint between the second solder ball 318 and the top surface and the second solder balls defines a distance between the melted first solder ball and the bottom surface.

In other words, claim 27 recites both (1) the first and second solder balls having different melting temperatures and (2a) the first solder ball creates the solder joint between the top surface

and the bottom surface and (2b) the second solder ball defines a distance between the top surface and the bottom surface. The combination of Burnette and Dockerty produces an invention that creates a solder joint between the top surface and the second solder ball and defines a distance between the melted first solder ball and the bottom surface. Therefore, Burnette and Dockerty fail to teach all of the limitations of the claimed present invention.

Regarding claims 18 and 19, it is submitted that the claims contain further patentable subject matter and are allowable not merely as being based on an allowable base claim.

Therefore, reconsideration and passage of claims 27 and 18-19 to issuance is respectfully requested.

Regarding claim 23, Applicants respectfully resubmit the above-offered position regarding the teachings of Burnette and Dockerty. As noted above, the combination of Burnette and Dockerty fail to teach or suggest (1) the soldering joint being created by the first solder balls, wherein the soldering joint is between the top surface and the bottom and (2) the defined minimum distance being between the carrier substrate and the printed circuit board based on the second solder balls. Rather, the combination of Burnette and Dockerty would create a system having a solder joint between the second solder balls and the top portion and the defined space between the melted first solder balls and the bottom portion. Therefore, one of ordinary skill in the art would not have combined these references because the combination thereof fails to teach or suggest the claimed present invention of claim 23.

Regarding claims 24-26, it is submitted that the claims contain further patentable subject matter and are allowable not merely as being based on an allowable base claim.

Therefore, reconsideration and passage of claims 23-26 to issuance is respectfully requested.

Added claims 28-31

As noted above, claims 28-31 recite a product by process claim, in accordance with MPEP §2173.05(p) reciting limitations previously found within existing claims 23-26.

Therefore, Applicants respectfully resubmit the above-offered position regarding the short-comings of the teachings of Dockerty and Burnette in view of the claimed limitations of the method steps of claim 23 and therefore the short-comings as applicable to the integrated circuit made by the same claimed process.

Therefore, as claim 23 –26 recite patentable limitations to a method for making an integrated circuit, the integrated circuit made by the process (as recited in claims 28-31) is therefore patentable. Furthermore, the underlying elements of the integrated circuit of claims 28-31 are patentable, as noted with respect to the discussion of pending claim 27. Passage of these claims to issuance is respectfully requested.

Accordingly, Applicant respectfully submits that the claims are in condition for allowance and that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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By: _____
Timothy J. Bechen
Registration No. 48,126

VEDDER, PRICE, KAUFMAN &
KAMMHOLZ, P.C.
222 N. LaSalle Street
Chicago, IL 60601
(312) 609-7500
FAX: (312) 609-5005